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Title: Design of Energy Efficient Power Amplifier for 4G User Terminals.

Publication year: 2010

Conference title: 17th IEEE International Conference on Electronics, Circuits, and Systems (ICECS 2010), Athens, Greece, 12-15 December, 2010.

Publisher: IEEE

Link to original published version: http://www.icecs2010.org/

Citation: Hussaini, A. S., Abd-Alhameed, R. A. and Rodriguez, J. (2010). Design of Energy Efficient Power Amplifier for 4G User Terminals. In: 17th IEEE International Conference on Electronics, Circuits, and Systems (ICECS 2010), Athens, Greece, 12-15 December, 2010. IEEE. ISBN: 978-1-4244-8156-9. Paper No. 533, pp. 617-620.

Design of Energy Efficient Power Amplifier for 4G User Terminals

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Abstract—**This paper describes the characterization and design of energy efficient user terminal transceiver power amplifier. To reduce the design of bulky external circuitry, the load modulation technique is employed. The design core is based on the combination of Class B and Class C that includes quarter wavelength transformer at the output to perform the load modulation. The handset transceiver for this power amplifier is designed to operate over the frequency range of 3.4GHz to 3.6GHz mobile WiMAX band. The performances of the load modulation amplifier are compared with conventional Class B amplifier. The results of 30dBm output power and 53% power added efficiency are achieved.**

Keywords-Class B; load modulation RF power amplifier; OFDM; mobile WiMAX

I. INTRODUCTION

The performance of the 4G handset transceiver depends primarily on the performance of RF power amplifier. However due the thirst high data rate of the 4G communications, it adopts OFDM modulation scheme. Certainly this scheme offers high data rate but is critically dependent on linearity of transceiver power amplifier due to its high crest factor. As a result of this phenomenon, the power amplifier mostly operates at the back off region and thus the resultant efficiency degrades dramatically. To boost the efficiency and keep the same margin for high crest factor signal, load modulation techniques with new offset line are employed.

A load modulation technique was proposed in 1936 [1] to work with AM broadcasting transmitter but at that time nobody adopted it. This was mainly because the signals of AM transmitter were around 0dBm crest factor. However, until recently beyond 2G where the transmission signals contains 8 to 12dBm crest factor and the load modulation becoming widely adopted. The concept of load modulation technique has been fully explained by the present authors of their previous work in [2]. The work involves the use of two or more power amplifiers with quarter wave transmission line coupler as an impedance inverting network. The resultant linear power amplifier achieved a higher efficiency at the outputs below peak output power (PEP) than conventional class B linear power amplifier [3], [4]. The technique essentially makes use of a Class C amplifier to adapt the load impedance at the Class AB amplifier for optimum efficiency over a wide range of output power. The quarter- wave transformers based on a transmission line structure are served as the power-coupling element between the two amplifier paths.

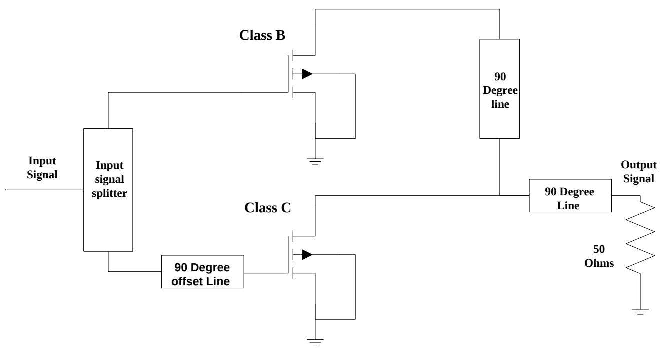

Figure 1. The schematic diagram of load modulation power amplifier

There are ten frequency bands defined in the WiMAX standard, the 3.5 GHz is the mobile WiMAX band and being the most common in Europe. This band has a range of frequency from 3.4GHz to 3.6GHz (Uplink: 3400MHz – 3500MHz, Downlink: 3500MHz – 3600MHz).

In this paper, the efficiency and the output power of the load modulation amplifier has been achieved by 1) Proposed additional of 32mm offset lines at the output and input matching network for which it prevents power leakage at the output junction between the output impedance transformer and peaking Class C amplifier, 2) The optimum design of Class B amplifier with proposed circuitry increases the quiescent current to an order of 8% of the peak drain current of the transistor, 3) The optimum design of the input signal of 3dB 90 degree splitter, and RF-DC blocking circuit proposed as an open short circuits are added to right angle of the RF blocking transmission lines. The schematic diagram is presented in Figure 1.

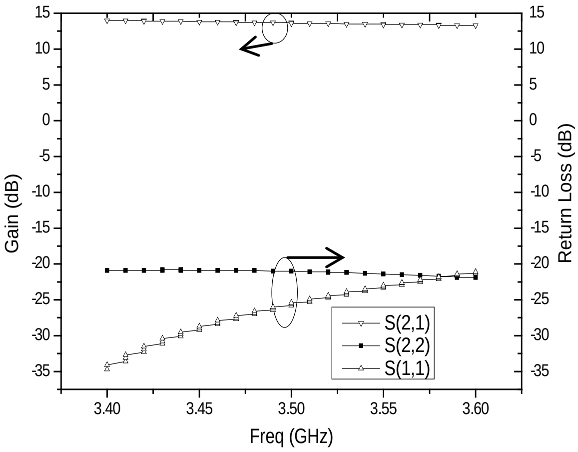

Figure 2. Linear simulation: Flat gain & return loss

II. CIRCUIT DESING

A 3.5GHz, 30dBm Mobile WiMAX handset load modulation RF power amplifier, has been designed using the TOM3 large signal model and FPD1500 transistor. The FPD1500SOT89 is a packaged depletion model AIGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT). It contains double recessed gate structure which minimizes parasitic and optimize performance.

This design comprised several design steps for which the optimization is applied to each in order to obtain global high performances of the entire load modulation RF power amplifier. Initially, the design of carrier and peak amplifiers, input 3dB 90 degree hybrid coupler designs, Output 90 degree offset line and impedance transformer designs were performed.

However, it is important to note that in the designing of carrier and peak amplifiers, the DC simulation should be done first in order to find the optimal bias point and bias network based on the class of operation and power requirements. In this paper the bias circuit was designed based on Class B and Class C of the carrier peaks. We decided to use class B to improve the efficiency and linearity instead of Class AB which is widely used in the combination of Doherty amplifier. The DC quiescent current for Class B is at threshold while for Class C is below the threshold. In theory the quiescent current of Class B is zero but for the current work, we increased the quiescent current to an order of 8% of the peak drain current that is resulting in 0.046mA. The reason for this is to minimize crossover distortion and increases the efficiency. The peak drain current is 0.587mA when the VGS is at 0V and VDS is 5V. 5V was chosen for VDS since it is located between cut-off and saturation of the transistor. 0.046mA is 8% of the peaks drain current which gave the VGS of -0.9V while the overall power consumption is 0.228Watts. Moreover, the same supplied power applied to class C but the drain current was 0.004mA and the power consumption was 0.019Watts.

Having obtained the DC quiescent current, the next step is to determine the load line impedance to design the output and input matching of Class B amplifier, to obtain the performance regarding the output power and efficiency. The output matching network was designed for optimum output power performance with load pull technique based on input matching S-parameters.

Figure 3. Power splitter

The transistor parasitic elements are included in the load-pull analysis in order to optimize the output matching network. The results obtained from the load pull simulation showed that the transistor needs to see an impedance of 20.492 + j3.775 at the output. Therefore the target of the matching network was to transform the impedance from 49.393 – j1.776 to 20.492 + j3.775. This impedance was the optimal load value which compromised the efficiency 40.39% and 27.05dBm output power at 1dB compression point of single Class B alone. The load reflection coefficient was used to design the output matching network while for the input matching network S-parameter was employed and conjugated the input reflection coefficient for maximum power transfer. Figure 2 shows the linear results obtained from matched Class B power amplifier, the gain is flat over the range of 3.4GHz to 3.6GHz with excellent matching at the input and output return losses.

The non-linear simulation of Class B was performed and the performance of the design in terms of output power and efficiency was observed. The 26.98dBm output power was achieved at 1dB compression point and 39% efficiency. From this nonlinear simulation, the result shows a clear compromise with the load pull measurement values. The same was applied to Class C but with different bias point.

A 3dB quadrature splitter is part of load modulation and if properly can contribute a lot to the total efficiency of the system. Our investigation shows that the operation of this technique is strongly influenced by the coupling factor of the input splitter. In fact, in this research 3dB quadrature splitter have been designed (Figure 3) and tested in terms the operated frequency and bandwidth, and this showed good results as appeared in Figures 4, and 5. It should be noted that, this splitter is at the input of amplifier will divides the input signal equally between the carrier and peaking amplifiers. The splitter, the Carrier Class B, the peaking Class C, and impedance transformer at the output are combined to form a load modulation RF power amplifier.

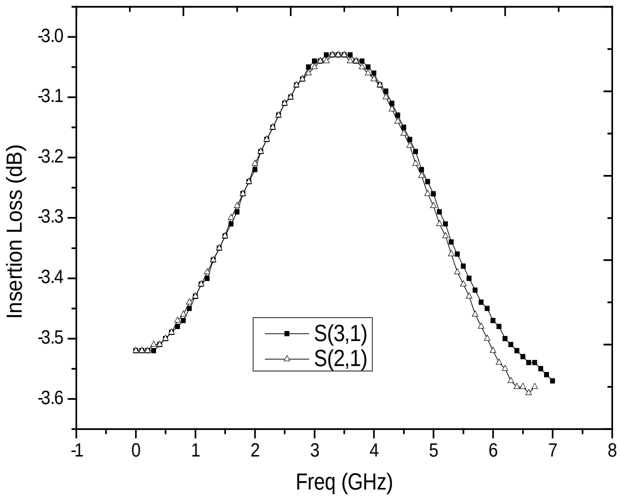

Figure 4. Insertion Loss

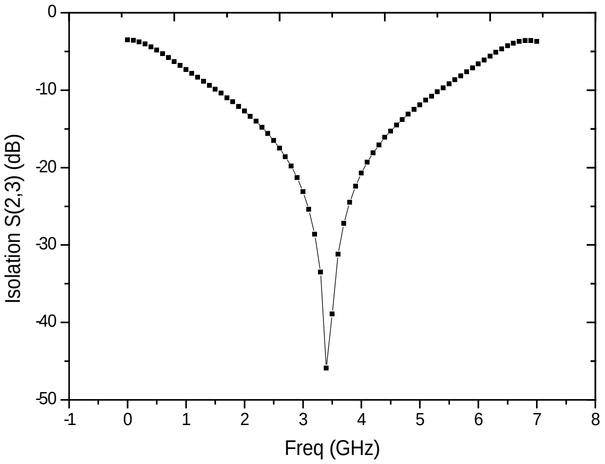

Figure 5. Isolation

III. Implementation & Results

Figure 6, shows the prototype diagram of the proposed load modulation RF power amplifier with offset transmission line at both output and input circuit which maximize the overall system's efficiency with the configuration of Class B amplifier. The FPD1500SOT89 transistor with 27.5dBm output power was used for both Class B and Class C amplifiers and produce a load modulation amplifier with 30dBm and Efficiency of 53%. Table 1 summarizes the recommended bias setting. The bias condition for the Class B carrier amplifier are Vgs = -0.9V (Ids = 46 mA), and for the Class C peaking amplifier, Vgs = -1.1V (Ids = 4 mA). Both of the amplifiers use the same drain voltage (5V)

The load modulation initially characterized for AM-AM and AM-PM responses as well as output power and efficiency. The performance comparisons between the load modulation amplifier and Class B amplifier are performed and the output power increased to 30dBm at 1dB compression point while the efficiency increased to 53%. Figure 7 represent the variation of the input power versus output power of the load modulation. It clearly shows that 30dBm output power is at linear region of the amplifier and this was achieved due to the characteristic of gain compression and expression of the load modulation. The peaking amplifier Class C late gain expansion can compensate the carrier Class B amplifier gain compression. Figure 9 represent the gain characteristic versus output power, the graph shows the power gain of load modulation amplifier is degraded drastically compared to Class B due to the arrangement of lower biasing.

Figure 10 shows the power added efficiency versus output power. The load modulation amplifier have higher efficiency over the range of wide output power levels compared to Class B amplifier.

Table 1: Bias point setting for load modulation

Drain Voltage	**Carrier VGS**	**Peaking VGS**
5V	-0.9V	-1.1V

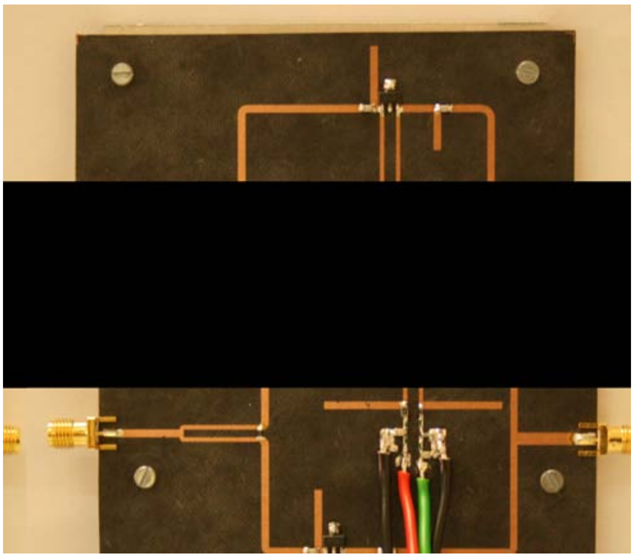

Figure 6. Implemented prototype of energy efficient 4G load modulation power amplifier

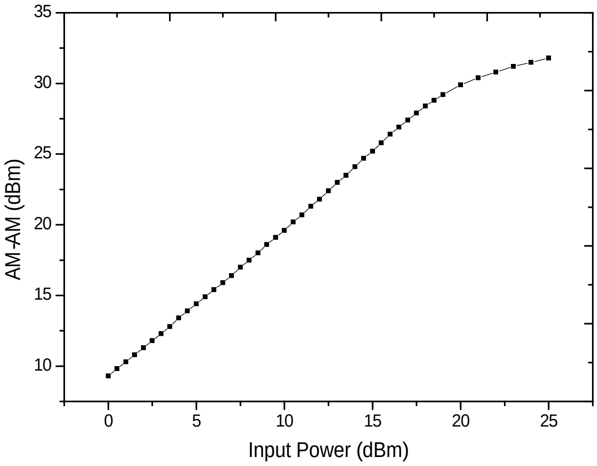

Figure 7. AM-AM characteristics of load modulation amplifier

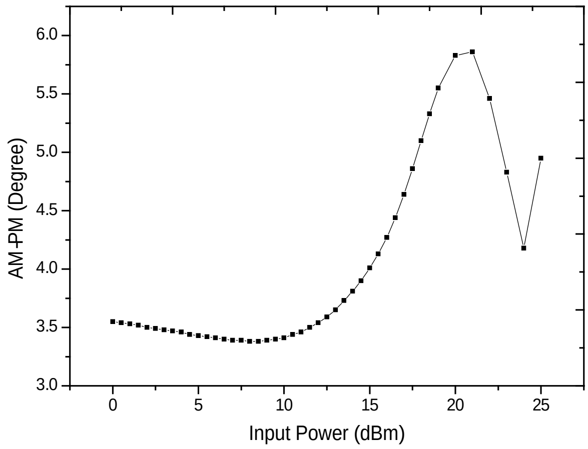

Figure 8. AM-PM characteristics of load modulation amplifier

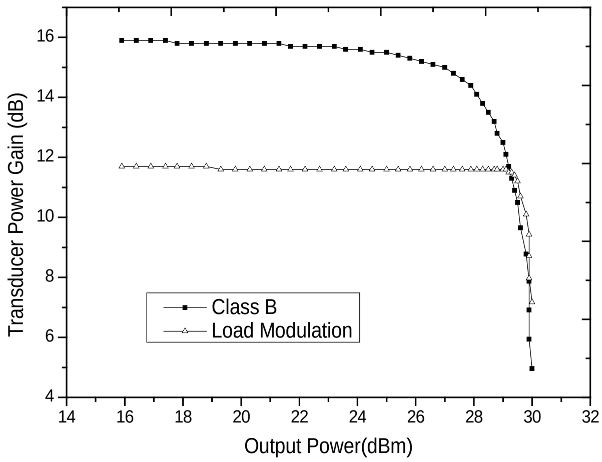

Figure 9. Gain characteristics

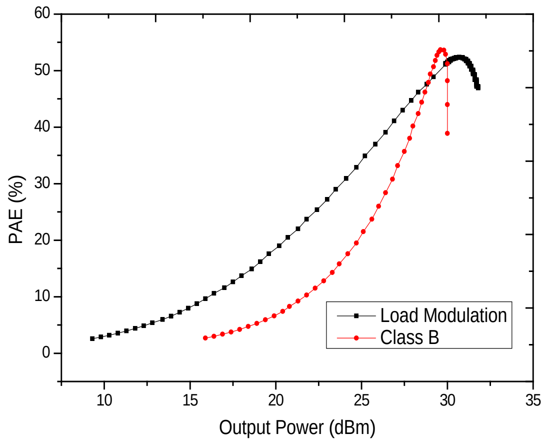

Figure 10. Power-Added Efficiency

Table 2: Comparison performance of Class B and Load modulation at Pout 1dB compression point

Amplifier	**Gain (dB)**	**Pout (dBm) at 1dB**	**PAE (%) at P1dB**
Class B amplifier	15.4dB	27.5dBm	37%
Load modulation	11.8dB	30dBm	53%

IV. Conclusion

The trade-off between efficiency and linearity in load modulation power amplifier has been presented. The achieved results of the proposed design process have shown an excellent efficiency and power performances. The proper phasing of 3dB quadrature splitter effectively contributed to the total efficiency of the system. The operation of this design was strongly influenced by the coupling factor of the splitter, biasing of class B and C amplifiers. In addition, the turn–on of the class C amplifier was dependent on the gate bias voltage and the input signal. The self-managing characteristic of the load modulation amplifier has made its implementation more attractive.

Acknowledgment

This work has been performed in the framework of the MOBILIA project (CP5-016) under the Eureka Celtic Framework, funded through the QREN Framework – PO Centro (project n. 5555).

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