Explanation of DC/RF Loci for Active Patch Antennas

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Abstract. A characteristic loop locus of dc power versus RF output power was observed as the frequency was varied around the optimum point of an operational active antenna. A new technique was introduced into the simulation, plotting the dependence of parameters such as supply current, efficiency or output power on internal impedance as seen by the naked transistor. It is now clear that the loop was formed as a consequence of the interaction of the transistor packaging elements with the patch impedances

Keywords: Active antenna, power amplifier, DC and RF power, patch antenna.

1 Introduction

A characteristic loop behaviour is observed in the DC input power – RF output power plane as the frequency is swept at a constant input drive level for an active rectangular patch radiator. Figure 1 shows some typical loops measured for the plain patch at different power levels. These results were obtained using our novel experimental test-bench arrangement described in [1,2]. This pattern was found to be true for all patch loads [2], shown in Figure 2a, regardless of their precise configuration. Therefore it is desirable to have a clear qualitative understanding of the dominant physical effects giving rise to this behaviour. Also the approximate shape (Figure 6) of the observed loop was predicted using the ADS circuit simulator.

2 Investigation by Simulation.

At first a simplified version of the circuit was analyzed using the medium power MLE531 MESFET transistor. It made very little difference to the loop structure whether the transistor was driven directly from a 50Ω source or a voltage source. Under both cases, internal feedback can only affect the gate voltage of the transistor

via the internal parasitic components (including both the intrinsic transistor and its associated packaging).

These tests suggested that feedback effects do not play a major role in the formation of the loops, or indeed the operation of the transistor in general. Simulations with harmonic load impedances set to zero do not appear to have very much effect on the shape of the loop. This is consistent with the experimental observation that different patch types with similar fundamental impedances produce similar loci.

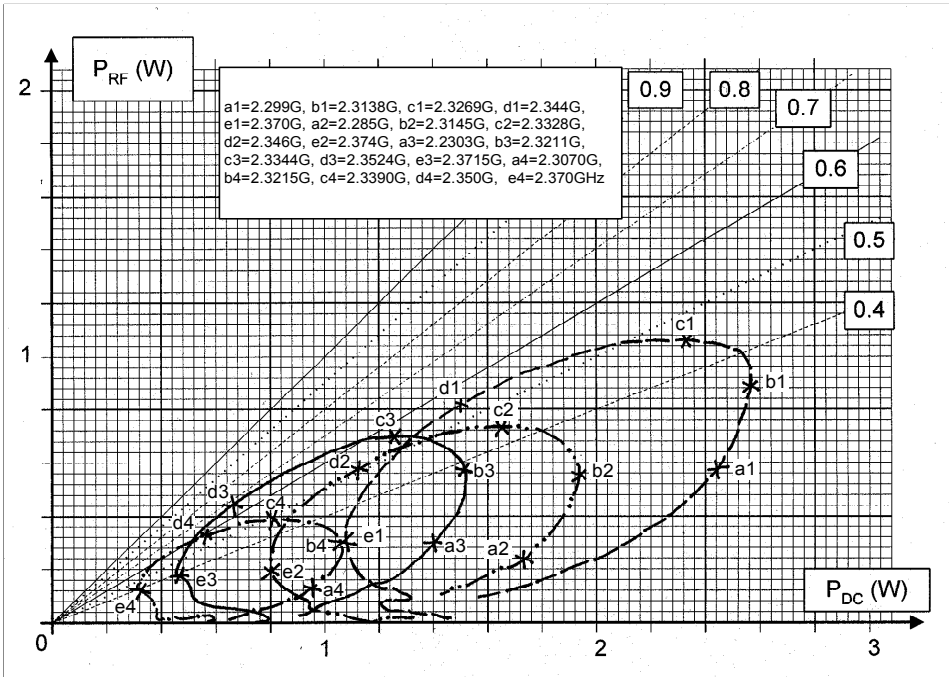
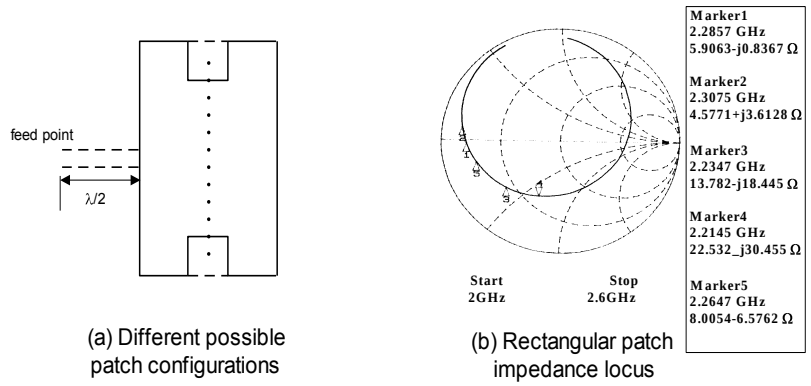


Figure 1: DC power/RF power loops generated experimentally for rectangular patch radiator



(a) Different possible patch configurations

(b) Rectangular patch impedance locus

Figure 2 Various used patch shapes for active antenna.

The attention was now turned to the packaging components of the transistor on the drain side. The ADS simulator permits the packaging components of the transistor to be simply disconnected, effectively reducing the device to an intrinsic or unpackaged transistor. Nevertheless, a significant element in the model, the shunt capacitor C_{DS} (Drain-Source), was still present in the intrinsic device. This may be cancelled out by inserting a capacitor of nearly equal negative value between drain and source. The model is now simplified further and the intrinsic transistor is close to the ideal case. This provides a simple starting point for explaining the effects of the load impedance.

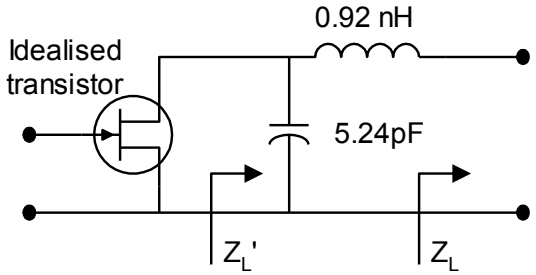


Figure 3: simplified simulation model

The transistor model is cascaded at its output with the shunt capacitor C_{DS}, and then with a short section of transmission line with a characteristic impedance of 35Ω and an electrical length of 9° at 1 GHz. It is considered reasonable to replace this transmission line with a series inductor, at least at the fundamental frequency of 2.35 GHz, of 13.5Ω reactance and an equivalent inductance of 0.92 nH. Since the shunt capacitor has a reactance of 12.9Ω, and 5.24pF capacitance, it is evident that both the capacitor and the inductor resonate at a frequency close to the design frequencies of the active patch. The transformation of the external load impedance Z_L to the value Z_L' seen by the ideal transistor is very marked, and approximates to an impedance inversion for small Z_L[1]. The second and third harmonics are above the resonant frequency of the LC network, and are subject to different, but still very significant transformations. The importance of these transformations was not fully addressed in [3-5], and the benefits of suppressing or moving the patch resonances near the second harmonic will require a more detailed analysis. In fact, it is obvious that the second harmonic impedance seen by the ideal transistor would be made zero by a capacitive external load chosen to series resonate with the packaging inductor.

The highly simplified model can now be employed to explain the formation of the DC – RF power loop. The DC current, RF (fundamental) power output, and DC/RF efficiency were plotted out as functions of the complex internal fundamental load impedance Z_L', with the internal harmonic impedances set to zero. The frequency was fixed at 2.334 GHz, the precise value is not critical since there are no longer any sharply resonant elements in the circuit. The incident drive power at the amplifier input was fixed at 26 dBm. Figure 4 shows the simulation DC current plot obtained.

[1] A short circuit external load will be transformed to an extremely high effective value as seen by the ideal transistor, because the L and C will then be in parallel resonance.

Plots of the RF output power and the DC/RF efficiency were both resemble figure 4 and hence were not included in this paper.

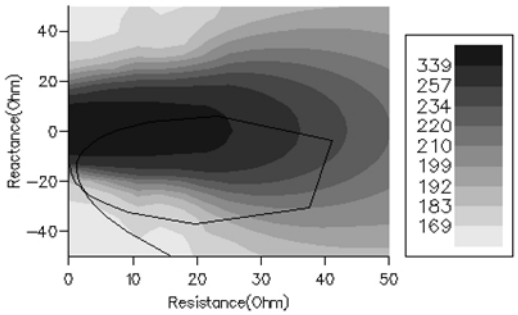


Figure 4: Simulated values of dc supply current versus fundamental load impedance, for idealized transistor

The near perfect symmetry of these plots about the zero reactance axis indicates that the internal feedback in the device is fairly small, and that with the output capacitance and packaging removed, we have an idealized device whose behaviour is fairly well explicable by its DC characteristics. The behaviour of the DC current plot is intuitively straightforward, in that increasing either resistance or reactance reduces the current, presumably by producing negative excursion of the drain voltage below its knee point.

The behaviour of the power dependence is also easy to visualize in the Z_L' plane as the power is given by $I^2 R_L'$, where I is the fundamental component of load current. A rough approximation could be made that this is proportional to the DC supply current in a nominal Class B operation with some error due to the distortion of the ideal Class B current waveform when R_L' and/or X_L' is large enough to cause current clipping. Figure 5 shows the output power dependency plotted as functions of the external impedance Z_L. It should be noted that this was obtained using the full transistor model.

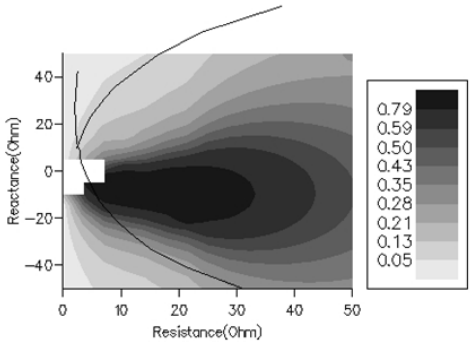


Figure 5 Simulated values of fundamental output power versus fundamental load impedance, for idealized transistor.

By tracing the locus of Z_L or Z_L' in the power/current contour plots as they are swept out with increasing frequency for a rectangular patch load, it is straightforward to predict the DC power/RF power loops. Figure 5 show the locus of Z_L, and this is a straightforward image of the patch's resonant loop as seen in the Smith chart of Figure 2b. Figure 4 show the corresponding locus of Z_L' which is Z_L transformed by the LC network only. The locus is totally different and now appears to show an additional resonance loop. The under sampling of points on this loop results from its extremely rapid frequency dependence. Figure 6 shows the power loops predicted by the two methods when the transistor is terminated with the rectangular patch. The loops obtained by both methods are quite similar, and comparable current/power values are obtained by the two methods at the same frequency. This shows that it is a fair approximation to neglect the source feedback effects and thus obtain a simple qualitative description of the effects.

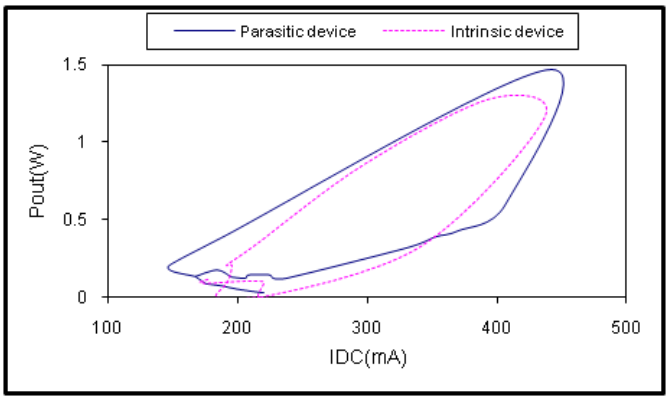


Figure 6 Simulated parasitic and intrinsic loops

3 Conclusions

It is seen that the formation of the loop is a consequence of the resonance effects caused by the interaction of the packaging L_D and C_{DS} with the resonant loop locus of the patch impedance. A critical range of Z_L values has a sufficiently low real part, and reactance, to series resonate with L_D to give very low impedances. As the reactance approaches zero there is a transition to parallel resonant behaviour. The rate of change of Z_L' in this frequency region is extremely rapid, and this explains why most of the DC – RF power loop is traced out over a much smaller frequency range than might be expected from the *Q* of the patch impedance resonance alone.

With the transformation to the internal impedance plane, a simple explanation has been given for the formation of the power loops. The initial fall in the magnitude of Z_L' accounts for the rapid rise in current and power, which both fall very rapidly on the top section of the loop as the rapidly rising impedance in parallel resonance chokes off the current.

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